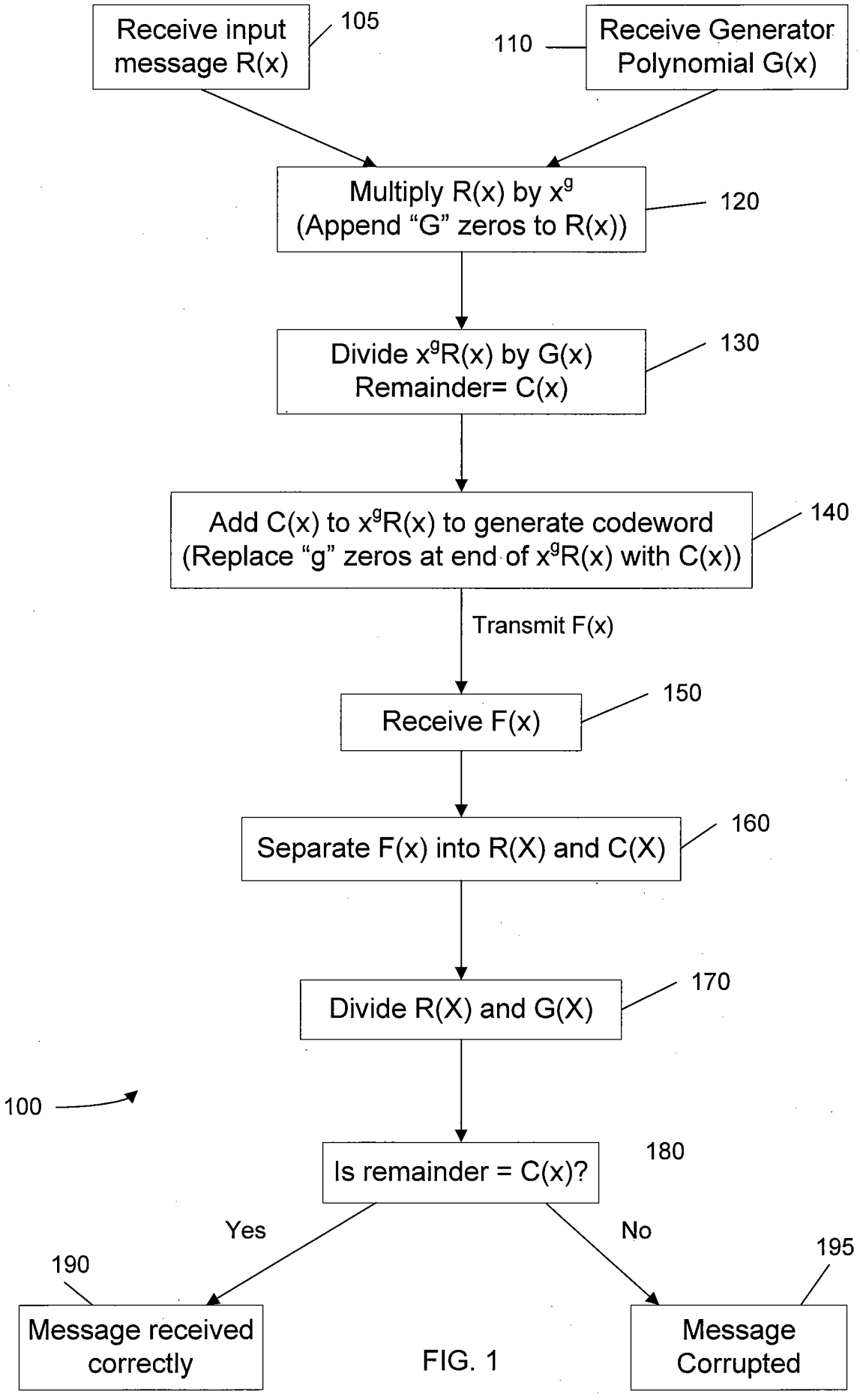

Receive input message R(x)
105
110
Receive Generator Polynomial G(x)
Multiply R(x) by x^g (Append "G" zeros to R(x))
120
Divide x^gR(x) by G(x) Remainder= C(x)
130
Add C(x) to x^gR(x) to generate codeword (Replace "g" zeros at end of x^gR(x) with C(x))
140
Transmit F(x)
Receive F(x)
150
Separate F(x) into R(X) and C(X)
160
Divide R(X) and G(X)
170
100
Is remainder = C(x)?
180
Yes
No
190
195
Message received correctly
Message Corrupted

FIG. 1

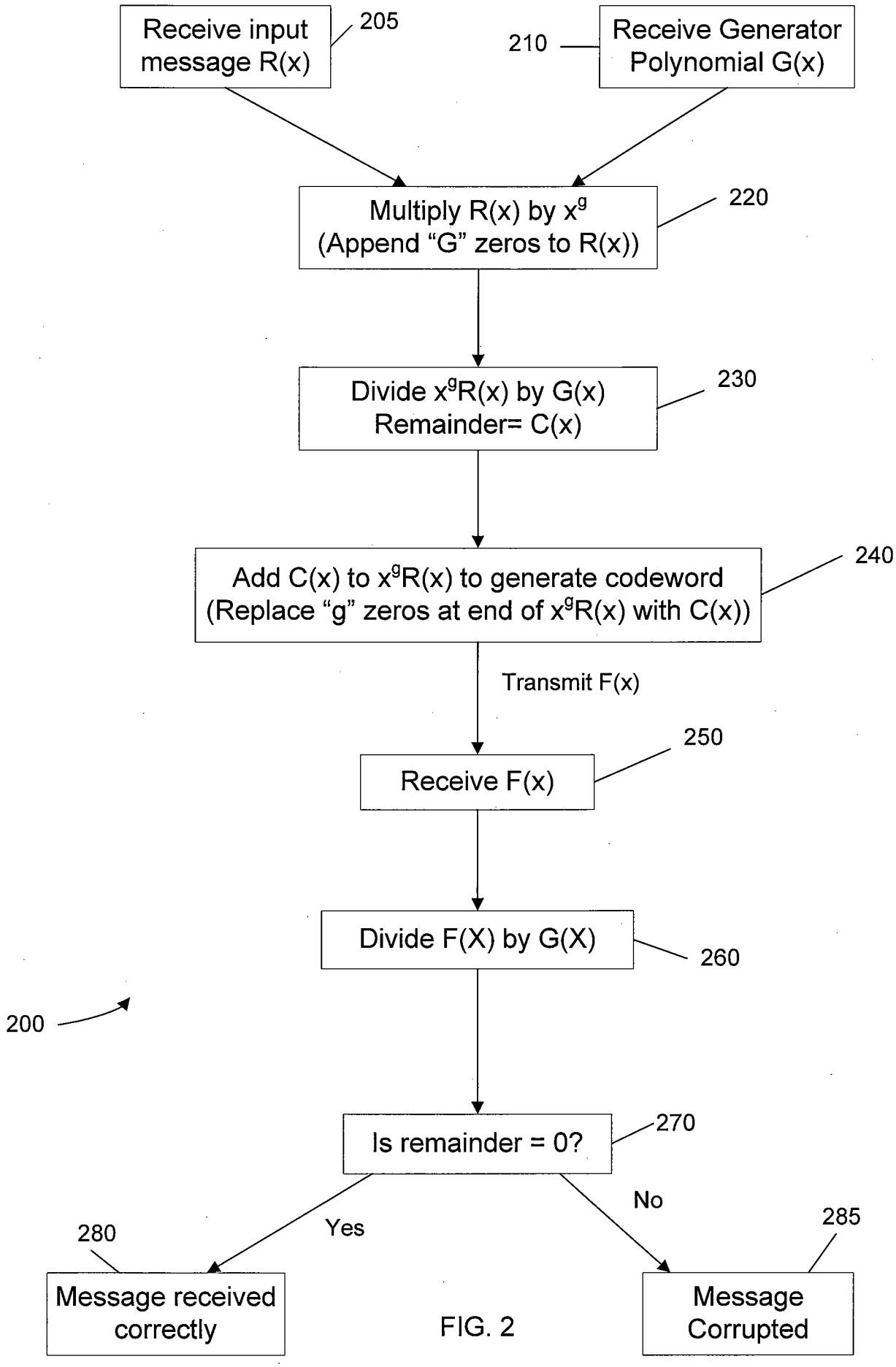

Receive input message R(x)
205
210
Receive Generator Polynomial G(x)
Multiply R(x) by x^g (Append "G" zeros to R(x))
220
Divide $x^gR(x)$ by G(x) Remainder= C(x)
230
Add C(x) to $x^gR(x)$ to generate codeword (Replace "g" zeros at end of $x^gR(x)$ with C(x))
240
Transmit F(x)
Receive F(x)
250
Divide F(X) by G(X)
260
200
Is remainder = 0?
270
Yes
No
280
285
Message received correctly
Message Corrupted

FIG. 2

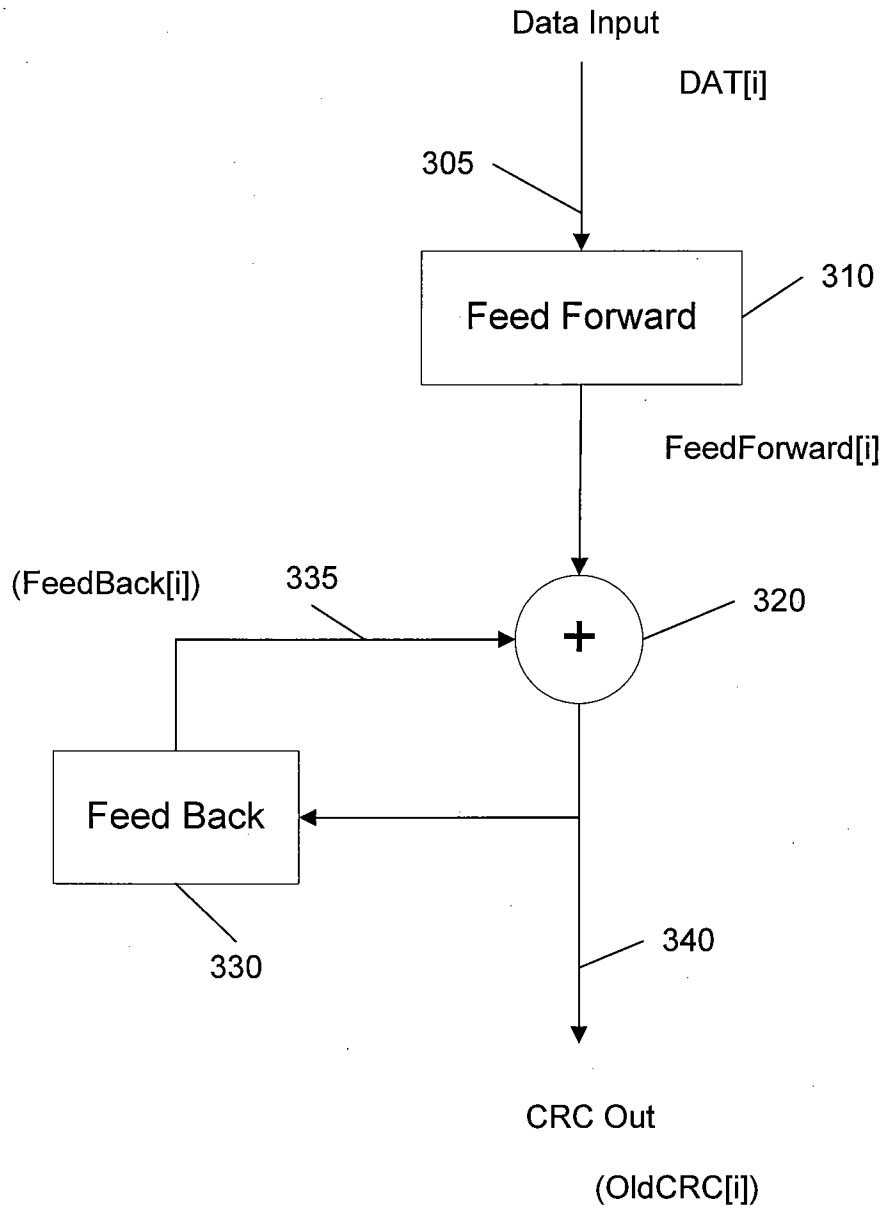
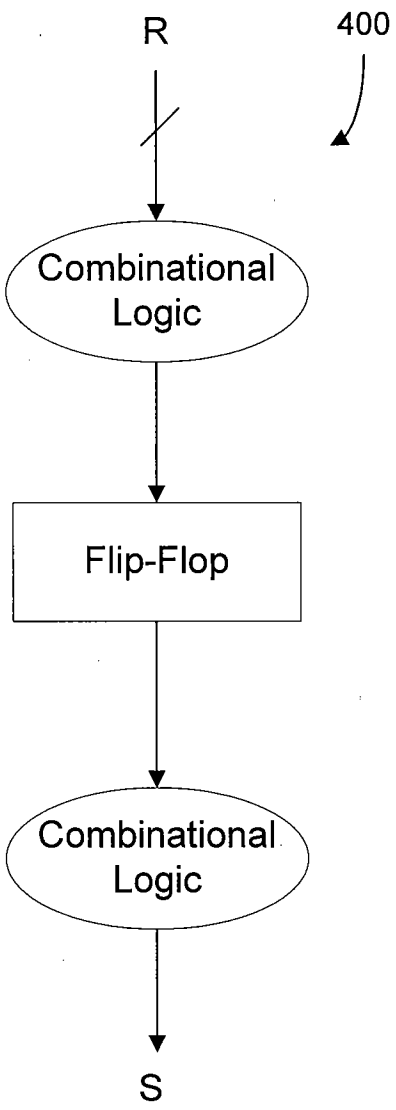
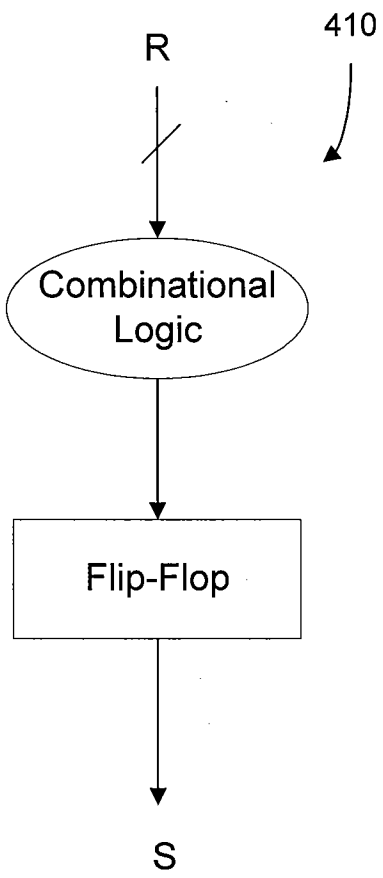
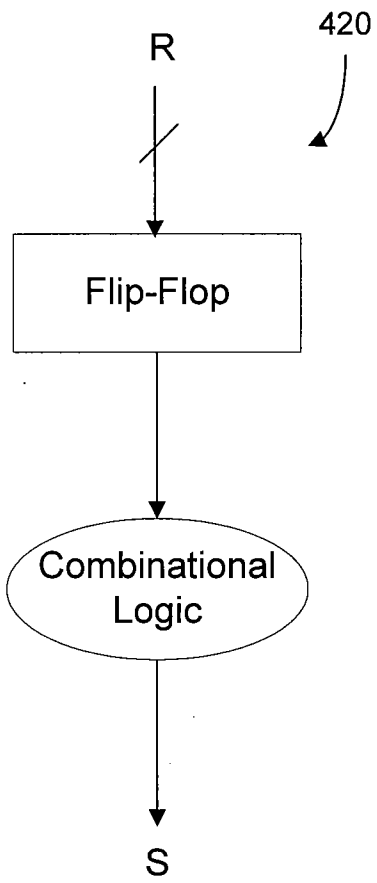

Data Input
DAT[i]
305
Feed Forward
310
FeedForward[i]
(FeedBack[i])
335
+
320
Feed Back
330
340
CRC Out
(OldCRC[i])

FIG. 3

FIG. 4


R
400
Combinational Logic
Flip-Flop
Combinational Logic
S


R
410
Combinational Logic
Flip-Flop
S


R
420
Flip-Flop
Combinational Logic
S

$$X^g(W_1\ W_2\ W_3) \bmod G = X^g(W_1 \bullet X^{2W} + W_2 \bullet X^W + W_3) \bmod G \sim 500$$

$$(W_1 \bullet X^{2W} + Z \bullet X^W + Z) \bmod G \sim 505$$

$$(Z \bullet X^{2W} + W_2 \bullet X^W + Z) \bmod G \sim 510$$

$$\frac{(Z \bullet X^{2W} + Z \bullet X^W + W_3) \bmod G \sim 515}{(W_1 \bullet X^{2W} + W_2 \bullet X^W + W_3) \bmod G \sim 520}$$

$$= \quad (W_1\ W_2\ W_3) \bmod G \sim 522$$

IF:
$$(W_1) \bmod G = S_1 \sim 530$$
$$(W_2) \bmod G = S_2 \sim 540$$
$$(W_3) \bmod G = S_3 \sim 550$$

THEN:
$$(S_1 \bullet X^{2W} + S_2 \bullet X^W + S_3) \bmod G \sim 560$$

$$= \quad (W_1 \bullet X^{2W} + W_2 \bullet X^W + W_3) \bmod G \sim 565$$

So:
$$(S_1 \bullet X^{2W} + Z \bullet X^W + Z) \bmod G \sim 570$$

$$(Z \bullet X^{2W} + S_2 \bullet X^W + Z) \bmod G \sim 575$$

$$\frac{(Z \bullet X^{2W} + Z \bullet X^W + S_3) \bmod G \sim 580}{(W_1 \bullet X^{2W} + W_2 \bullet X^W + W_3) \bmod G \sim 590}$$

$$= \quad (W_1\ W_2\ W_3) \bmod G \sim 595$$

FIG. 5

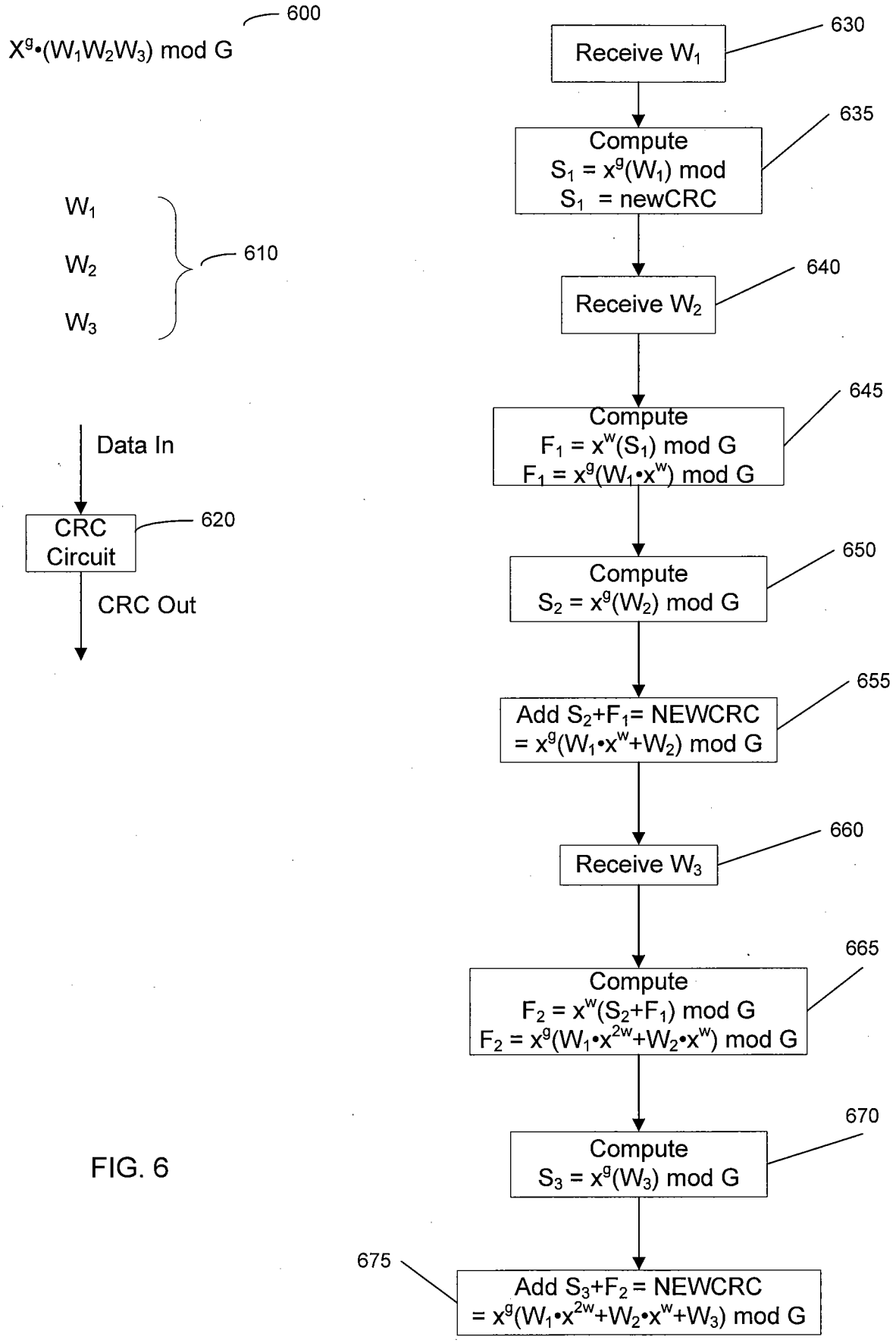

600
$X^g \cdot (W_1W_2W_3) \bmod G$
W_1
W_2
W_3
610
Data In
CRC Circuit
620
CRC Out
Receive W_1
630
Compute $S_1 = x^g(W_1) \bmod S_1 = \text{newCRC}$
635
Receive W_2
640
Compute $F_1 = x^w(S_1) \bmod G$ $F_1 = x^g(W_1 \cdot x^w) \bmod G$
645
Compute $S_2 = x^g(W_2) \bmod G$
650
Add $S_2+F_1 = \text{NEWCRC}$ $= x^g(W_1 \cdot x^w + W_2) \bmod G$
655
Receive W_3
660
Compute $F_2 = x^w(S_2+F_1) \bmod G$ $F_2 = x^g(W_1 \cdot x^{2w} + W_2 \cdot x^w) \bmod G$
665
Compute $S_3 = x^g(W_3) \bmod G$
670
675
Add $S_3+F_2 = \text{NEWCRC}$ $= x^g(W_1 \cdot x^{2w} + W_2 \cdot x^w + W_3) \bmod G$

FIG. 6

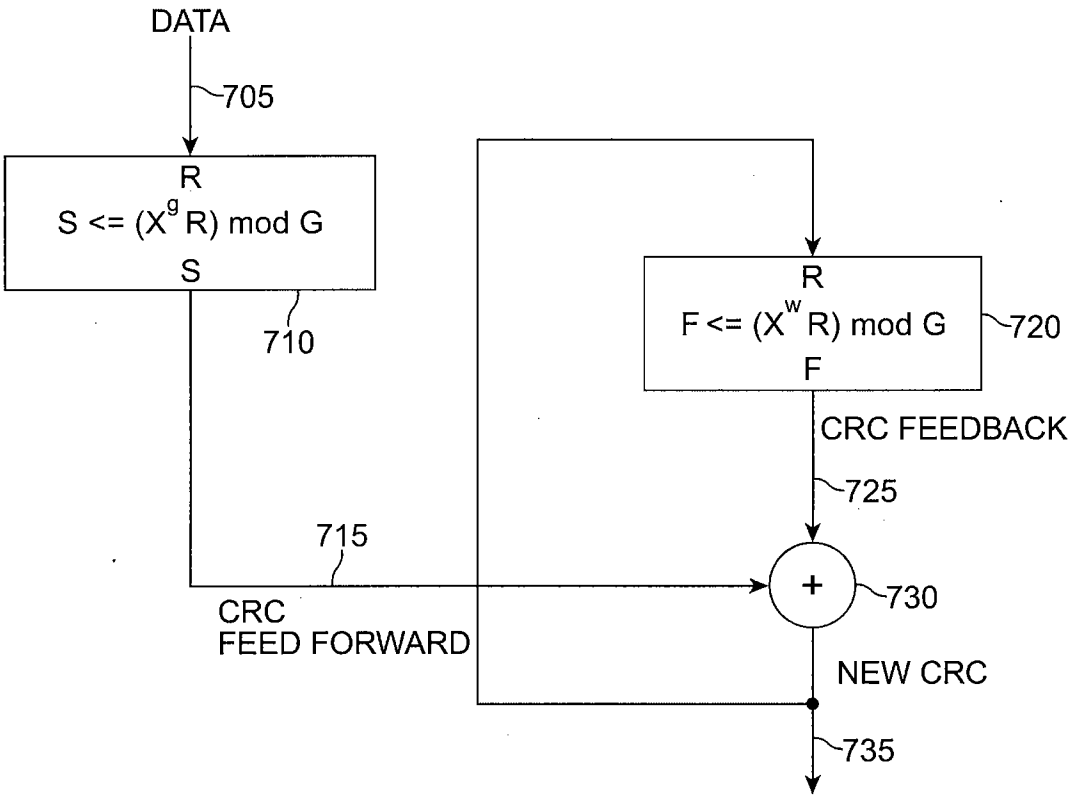

DATA
705
R
S <= (X^g R) mod G
S
710
R
F <= (X^w R) mod G
F
720
CRC FEEDBACK
725
715
CRC
FEED FORWARD
+
730
NEW CRC
735

FIG. 7

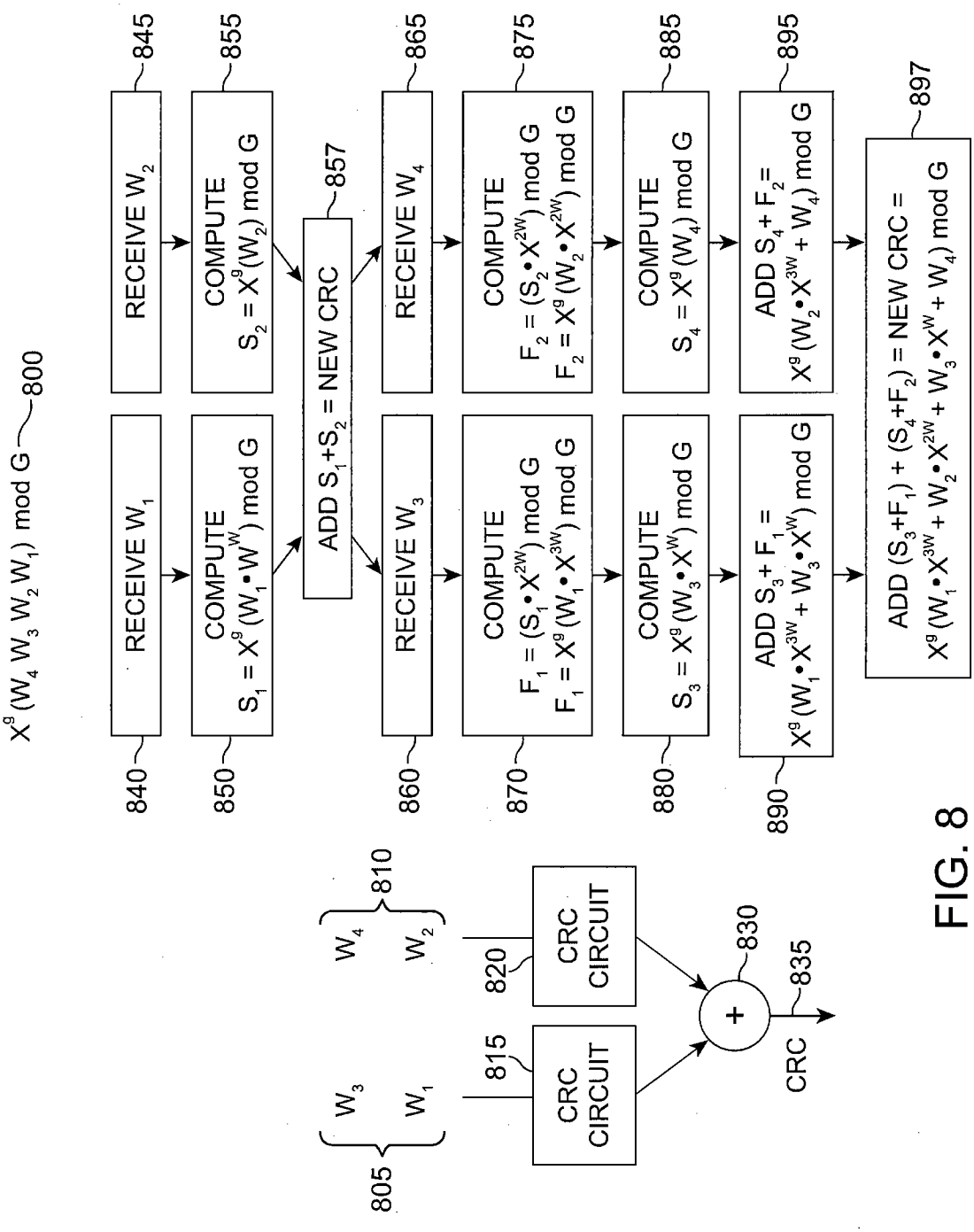

$X^g(W_4\ W_3\ W_2\ W_1)$ mod G
800
RECEIVE W_1
840
COMPUTE $S_1 = X^g(W_1 \bullet W^W)$ mod G
850
RECEIVE W_2
845
COMPUTE $S_2 = X^g(W_2)$ mod G
855
ADD S_1+S_2 = NEW CRC
857
RECEIVE W_3
860
COMPUTE $F_1 = (S_1 \bullet X^{2W})$ mod G
$F_1 = X^g(W_1 \bullet X^{3W})$ mod G
870
RECEIVE W_4
865
COMPUTE $F_2 = (S_2 \bullet X^{2W})$ mod G
$F_2 = X^g(W_2 \bullet X^{2W})$ mod G
875
COMPUTE $S_3 = X^g(W_3 \bullet X^W)$ mod G
880
COMPUTE $S_4 = X^g(W_4)$ mod G
885
ADD S_3+F_1 =
$X^g(W_1 \bullet X^{3W} + W_3 \bullet X^W)$ mod G
890
ADD S_4+F_2 =
$X^g(W_2 \bullet X^{3W} + W_4)$ mod G
895
ADD $(S_3+F_1) + (S_4+F_2)$ = NEW CRC =
$X^g(W_1 \bullet X^{3W} + W_2 \bullet X^{2W} + W_3 \bullet X^W + W_4)$ mod G
897
W_3 W_1
805
W_4 W_2
810
CRC CIRCUIT
815
CRC CIRCUIT
820
+
830
CRC
835

FIG. 8

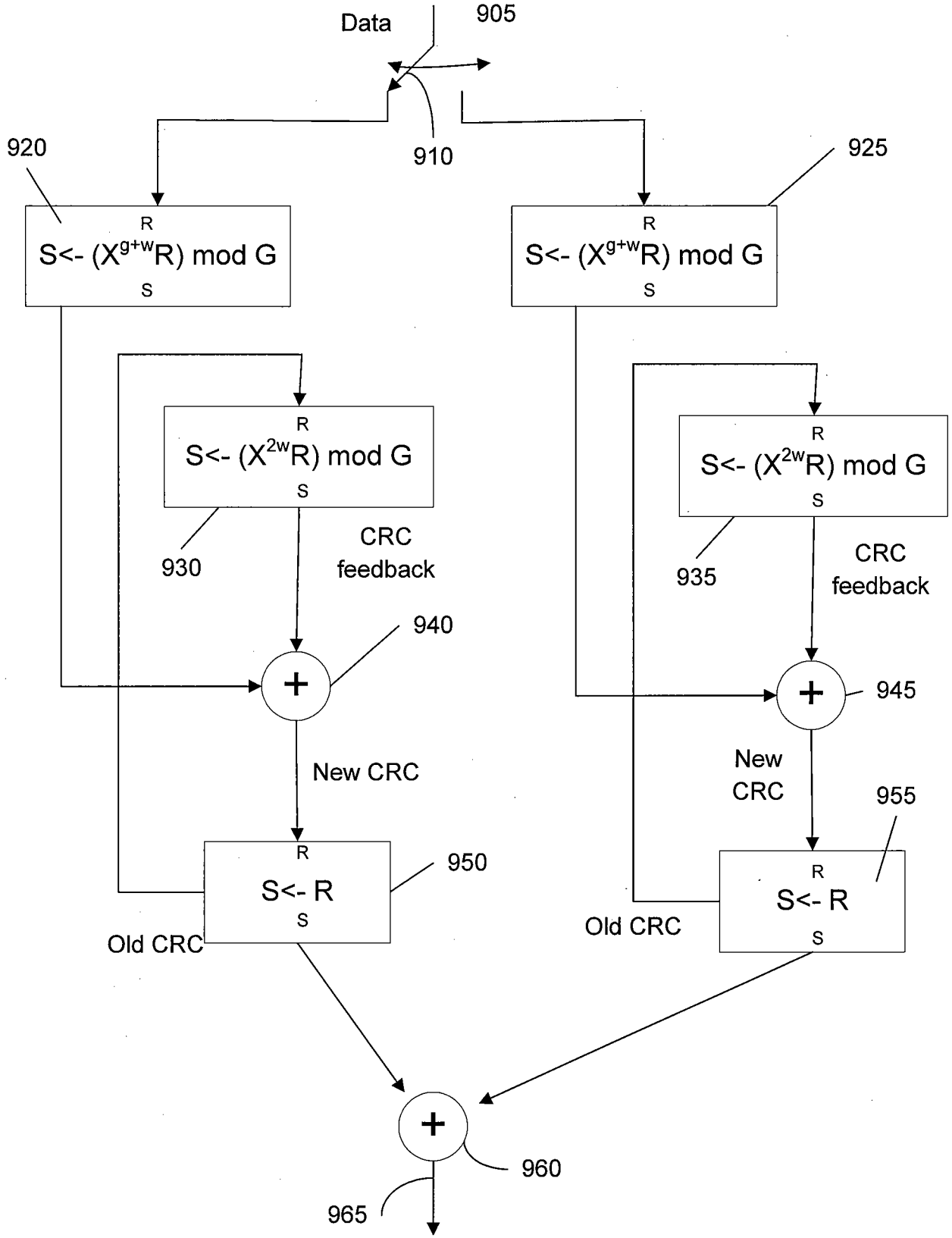

Data
905
910
920
925
R
S<- (X^{g+w}R) mod G
S
R
S<- (X^{2w}R) mod G
S
930
CRC feedback
935
940
945
+
New CRC
955
950
R
S<- R
S
Old CRC
960
965

FIG. 9

$$X^g(W_1\ W_2\ W_3) \bmod G = X^g(W_1 \bullet X^{2W} + W_2 \bullet X^W + W_3) \bmod G \quad 1010$$

$$(W_1 \bullet X^{2W} + Z \bullet X^W + W_3) \bmod G \quad 1015$$

$$\frac{(Z \bullet X^{2W} + W_2 \bullet X^W + Z) \bmod G \quad 1020}{(W_1 \bullet X^{2W} + W_2 \bullet X^W + W_3) \bmod G \quad 1025}$$

IF: $(W_1) \bmod G = S_1$ 1030

$(W_2) \bmod G = S_2$ 1035

$(W_3) \bmod G = S_3$ 1040

THEN: $(S_1 \bullet X^{2W} + Z \bullet X^W + S_2) \bmod G$ 1045

$$\frac{(Z \bullet X^{2W} + S_2 \bullet X^W + Z) \bmod G \quad 1050}{(W_1 \bullet X^{2W} + W_2 \bullet X^W + W_3) \bmod G \quad 1055}$$

$= (W_1\ W_2\ W_3) \bmod G$ 1060

FIG. 10

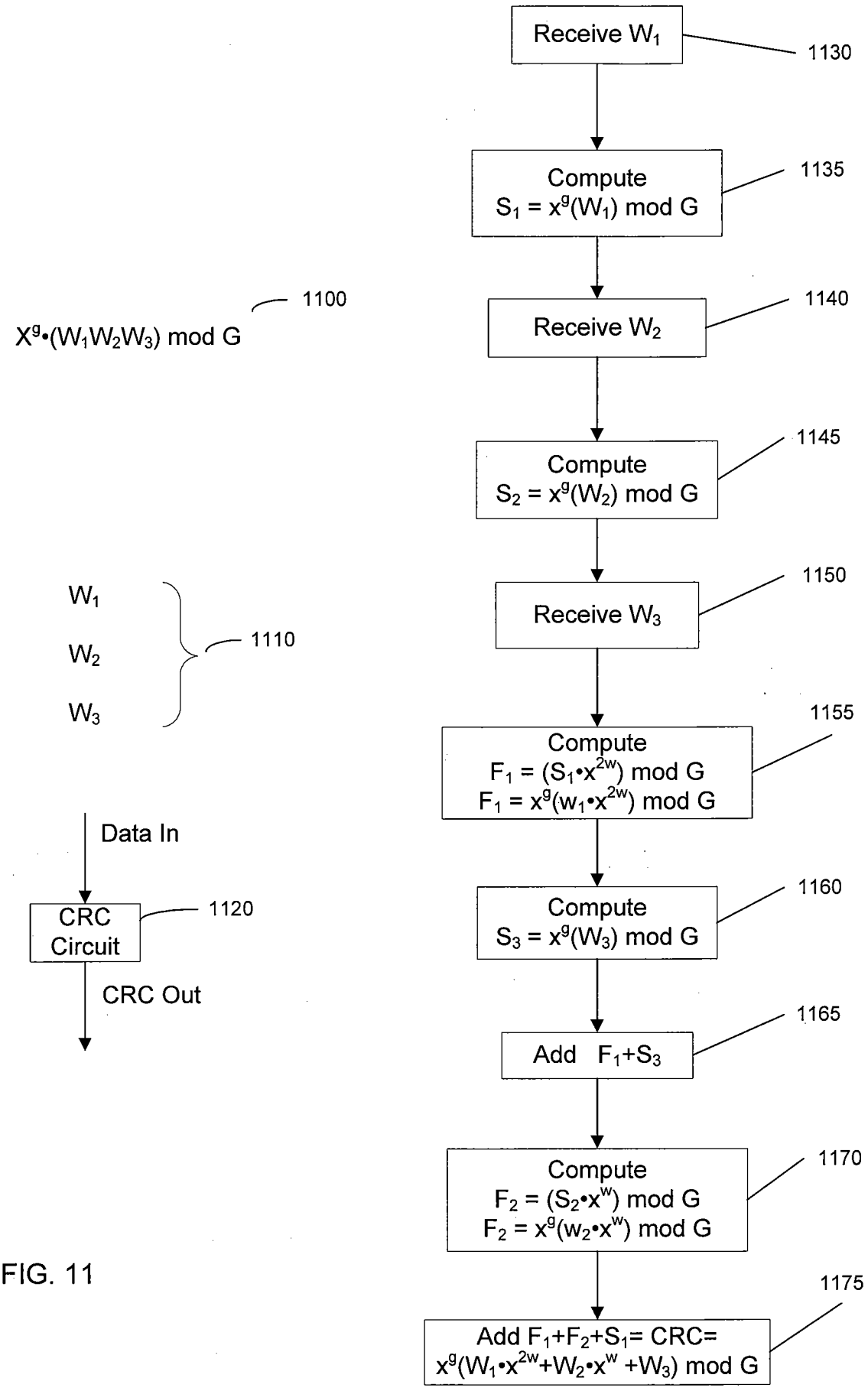

1100
$X^g \cdot (W_1W_2W_3) \bmod G$
W_1
W_2
W_3
1110
Data In
CRC Circuit
1120
CRC Out
Receive W_1
1130
Compute $S_1 = x^g(W_1) \bmod G$
1135
Receive W_2
1140
Compute $S_2 = x^g(W_2) \bmod G$
1145
Receive W_3
1150
Compute $F_1 = (S_1 \cdot x^{2w}) \bmod G$ $F_1 = x^g(w_1 \cdot x^{2w}) \bmod G$
1155
Compute $S_3 = x^g(W_3) \bmod G$
1160
Add F_1+S_3
1165
Compute $F_2 = (S_2 \cdot x^w) \bmod G$ $F_2 = x^g(w_2 \cdot x^w) \bmod G$
1170
Add $F_1+F_2+S_1$= CRC= $x^g(W_1 \cdot x^{2w}+W_2 \cdot x^w+W_3) \bmod G$
1175

FIG. 11

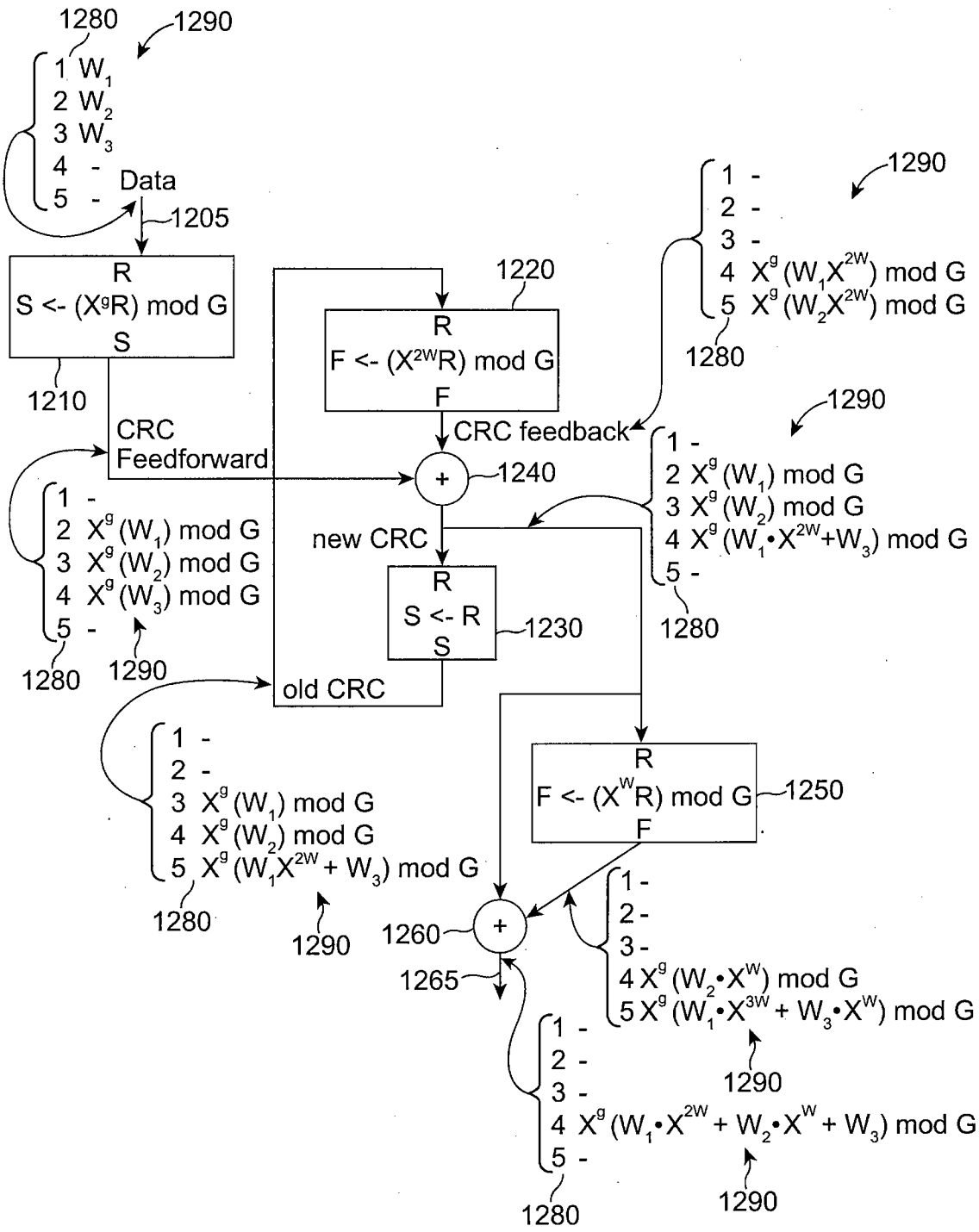

1280
1290
1 W1
2 W2
3 W3
4 -
5 -
Data
1205
R
S <- (XgR) mod G
S
1210
1220
R
F <- (X2WR) mod G
F
CRC feedback
1 -
2 -
3 -
4 Xg (W1X2W) mod G
5 Xg (W2X2W) mod G
1280
1290
CRC Feedforward
+
1240
1 -
2 Xg (W1) mod G
3 Xg (W2) mod G
4 Xg (W3) mod G
5 -
1280
1290
new CRC
R
S <- R
S
1230
1 -
2 Xg (W1) mod G
3 Xg (W2) mod G
4 Xg (W1•X2W+W3) mod G
5 -
1280
old CRC
R
F <- (XWR) mod G
F
1250
1 -
2 -
3 Xg (W1) mod G
4 Xg (W2) mod G
5 Xg (W1X2W + W3) mod G
1280
1290
1260
+
1265
1 -
2 -
3 -
4 Xg (W2•XW) mod G
5 Xg (W1•X3W + W3•XW) mod G
1290
1 -
2 -
3 -
4 Xg (W1•X2W + W2•XW + W3) mod G
5 -
1280
1290

FIG. 12

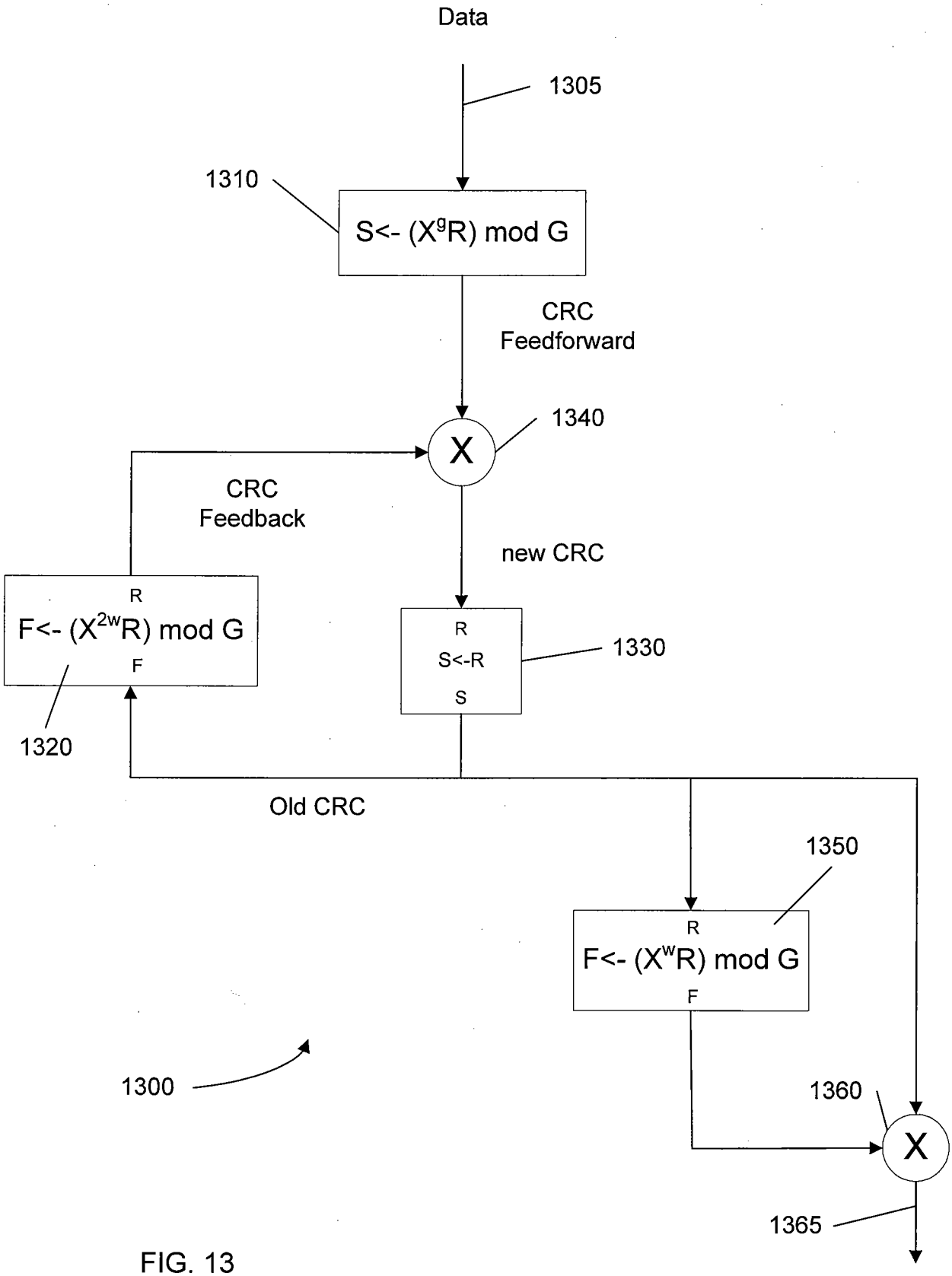

Data
1305
1310
S<- (X^gR) mod G
CRC
Feedforward
1340
X
CRC
Feedback
new CRC
R
F<- (X^2wR) mod G
F
R
S<-R
S
1330
1320
Old CRC
1350
R
F<- (X^wR) mod G
F
1300
1360
X
1365

FIG. 13

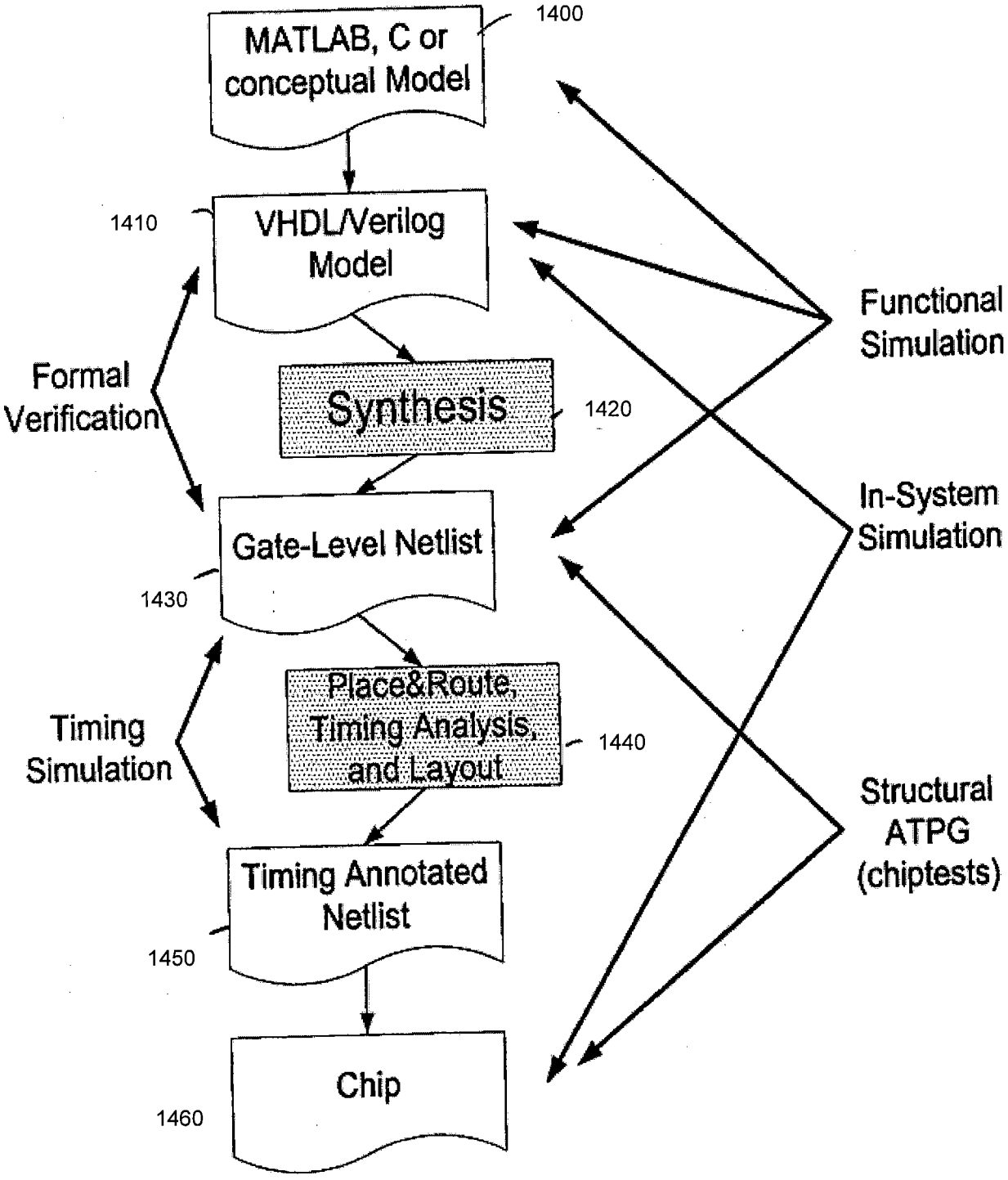

MATLAB, C or conceptual Model
1400
VHDL/Verilog Model
1410
Synthesis
1420
Gate-Level Netlist
1430
Place&Route, Timing Analysis, and Layout
1440
Timing Annotated Netlist
1450
Chip
1460
Formal Verification
Timing Simulation
Functional Simulation
In-System Simulation
Structural ATPG (chiptests)

FIG. 14

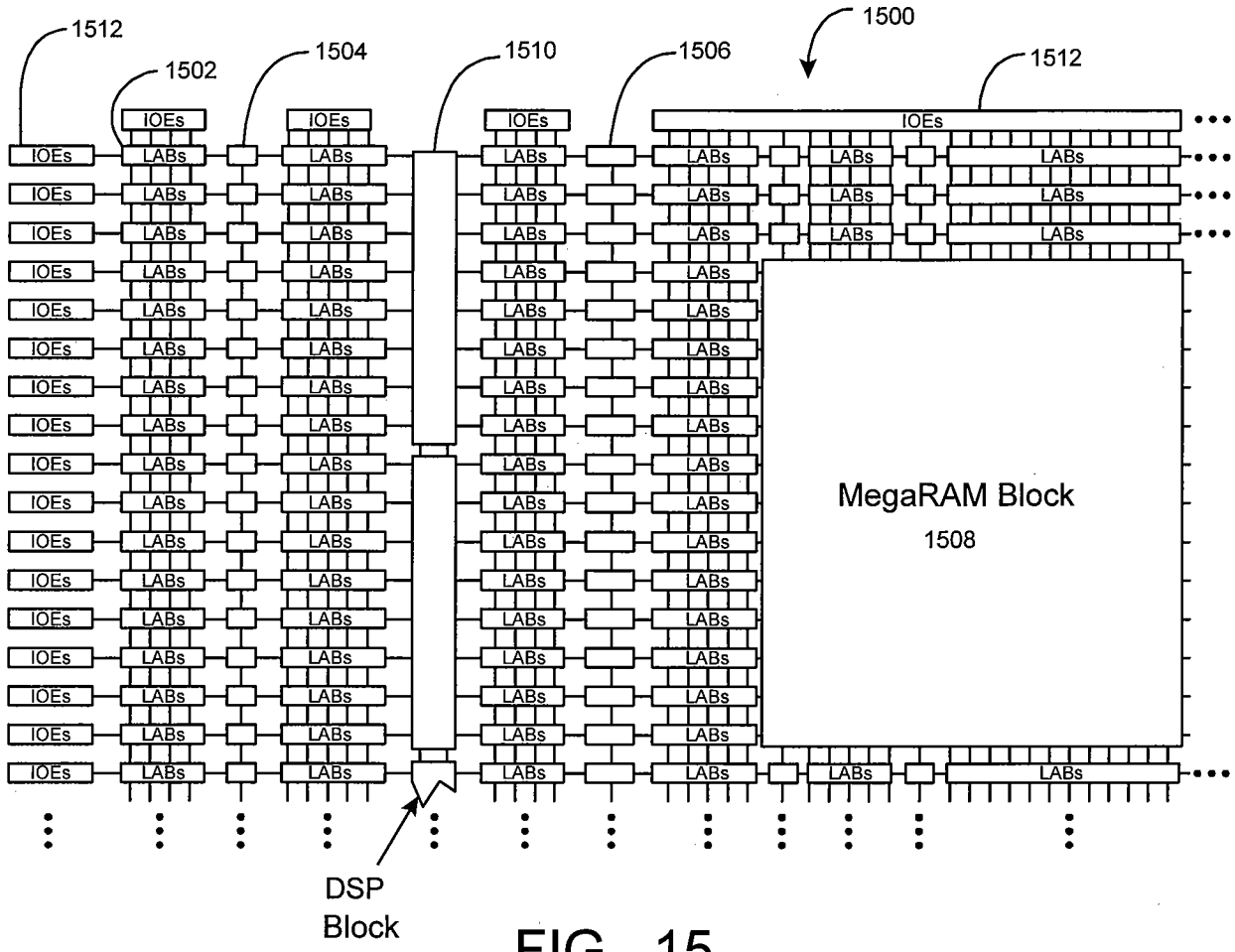

1512
1502
1504
1510
1506
1500
1512
IOEs
LABs
MegaRAM Block
1508
DSP
Block

FIG. 15

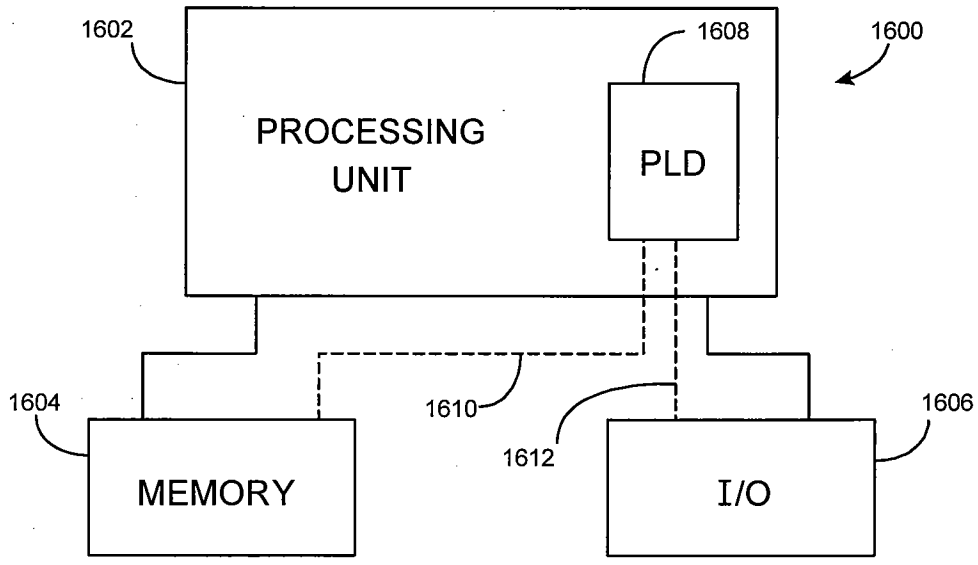

1602
1608
1600
PROCESSING
UNIT
PLD
1604
1610
1612
1606
MEMORY
I/O

FIG. 16